REMARKS

Claims 1-27 are pending in the above-referenced patent application. (Claims 28-42 were withdrawn from consideration by the Examiner and have been canceled).

Claims 1-27 were rejected. Specifically, Claims 1, 3, 5-10, 12-27 were rejected under 35 U.S.C. 103(a) as being unpatentable over US APP 2002/0081873 to Harris et al ("Harris") in view of USPN 6,763,402 to Talati. Claims 2, 4, 11 were rejected under 35 U.S.C. 103(a) as being unpatentable over Harris, in view of Talati and further in view of USPN 6,131,135 to Abramson et al. ("Abramson"). The rejections are essentially for the same reasons as in the reasons provided by the Examiner in the previous office action. All of the rejections are respectfully traversed because, for at lese the following reasons, the references, alone or in combination, do not disclose all of the limitations of the claims. Further, no prima facie case of obviousness has been established by the Examiner.

Interview Summary

Applicant wishes to thank the Examiner for the courtesies shown to the undersigned during the phone interview of March 23, 2006, between the undersigned and Examiner Nimesh Patel. In the interview rejection of Claim 1 in view of Harris and Talati were discussed. The undersigned argued that Harris and/or Talati do not teach, suggest or motivate connecting multiple USB-to-IDE bridges to a USB controller via a USB bus, as claimed. The undersigned further traversed the Examiner's statement in paragraph 35 (page 9) of the office action, and specifically traversed the Examiner's conclusion that motivation of combining Harris and Talati is "in the knowledge generally available to one of ordinary skill in the art", as not substantiated in the Office Action and that burden of proof under 35 USC 103(a) is not met by the Examiner. The undersigned further stated that Harris only shows a mass storage circuit board that carries the bridge chip 100 and disk drive *electronics* (not a storage device itself, such as disk drive, as in claim 19). In response the Examiner essentially repeated the arguments in the office action. No agreement was reached.

Rejections of Claims 1, 3, 5-10, 12-27 Under 35 USC 103(a)

All of the rejections are respectfully traversed because, for at lese the following reasons, the references, alone or in combination, do not disclose all of the limitations of the claims. Further, no prima facie case of obviousness has been established.

Harris is directed to a bridging circuit that is configured to provide communication between a mass storage device motherboard and a USB port on a host motherboard.

As per **Claim 1**, Harris does not disclose plurality of bridges per USB controller. As the Examiner also states, unlike the claimed invention herein, Harris does not disclose multiple bridges connected to a USB controller. Harris only mentions and shows that a mass storage device motherboard or secondary board includes a bridging Circuit. One mass storage device, is connected to one bridge.

Harris does not mention: "a USB controller, wherein the USB-to-IDE bridges are connected to the USB controller via a USB bus". Harris does not disclose a USB controller that is connected to multiple USB-to-IDE bridges via a USB bus for communication therewith.

Further, Harris does not disclose a USB controller, wherein the USB-to-IDE bridges are connected to the USB controller via the USB bus, such that a processor can communicate with the IDE devices via the USB controller.

There is no motivation suggested by either reference to combine them. It is well settled that in order for a modification or combination of the prior art to be valid, the prior art itself must suggest the modification or combination, "...invention cannot be found obvious unless there was some **explicit** teaching or suggestion in the art to motivate one of ordinary skill to combine elements so as to create the same invention." *Winner International Royalty Corp. v. Wang*, No. 96-2107, 48

USPQ.2d 1139, 1140 (D.C.D.C. 1998) (emphasis added). "The prior art **must provide** one of ordinary skill in the art the **motivation** to make the proposed molecular modifications needed to arrive at the claimed compound." *In re Jones*, 958 F.2d 347, 21 USPQ.2d 1941, 1944 (Fed. Cir. 1992) (emphasis added).

Harris provides no motivation or suggestion for connecting multiple bridges to a USB controller. Indeed, the Examiner has interpreted the claimed limitation as mere duplication of working parts of the USB-to-IDE bridge, which is coupled to an IDE device, requiring only routine skill in the art. Applicant respectfully disagrees. If that was indeed the case, at least Harris would have mentioned the advantages of connecting multiple USB-to-IDE bridges to a USB controller.

The Examiner relies on Talati (Fig. 1) to disclose plurality of bridges to connect plurality of IDE devices. Then, the Examiner concludes that it would have been obvious to use plurality of USB-to-IDE bridges connected to a respective IDE device since this would enable multiple IDE devices to be connected to the host using the USB interface and increase storage capacity.

Talati (Fig. 1, relied on by the Examiner) only shows DSD devices 110-112 connected to respective bridges 120-122, and bridges 120-122 connected to PHY controller 102. However, Talati does not indicate anywhere that the bridges do any kind of translation that even relate Talati to translation function in bridge of Harris. Talati states that the bridge 120 is a bridge chip 160 that implements a connection to the serial bus 14 by providing a PHY layer protocol controller 170 and a link layer protocol controller 172. As such, the bridge chip is totally unlike the chip 100 of Harris (FIG. 4).

Applicant traverses the Examiner's conclusion that motivation of combining Harris and Talati is in the knowledge generally available to one of ordinary skill in the art.

The Examiner does not met the burden under 35 USC 103(a) of showing how DSD bridges 120-122 in Talati are in any way even compatible with Harris's USB system.

The Examiner has not met the burden under 35 USC 103(a) of showing how DSD bridges 120-122 in Talati, that implement a connection to the serial bus 14 by providing a PHY layer protocol controller 170 and a link layer protocol controller 172, can be used to modify Harris's USB system to achieve the claimed limitations without need for extensive redesign of Harris.

The Examiner has not met the burden under 35 USC 103(a) of showing why one of ordinary skill in the art would consider Talati which mentions DSD bridges to modify Harris which is directed to a bridging circuit that is configured to provide communication between a mass storage device motherboard and a USB port on a host motherboard. What does DSD have to do with USB?

Further, simply because there may be general need to increase storage capacity (as the Examiner states), this does not require use of a plurality of IDE devices, and a plurality of USB-to-IDE bridges, wherein each IDE device is connected to a respective USB-to-IDE bridge, as claimed herein. For example, in Harris, for more capacity, a larger disk drive can be used rather than multiple bridges and IDE devices.

In case of Harris this is specially the case since Harris is concerned with integration to eliminate cables, power usage, EMI emissions (see e.g. paragraph 27). As such, indeed Harris teaches away from using multiple disk drives and bridges, as claimed. Indeed, despite the Examiner's reasoning, Harris motivates one of ordinary skill in the art who may need more storage, to not use multiple hard drives with associated cables, clutter, power usage, space usage, etc., and rather just obtain a larger disk drive to connect to the board 20a, and save USB ports. As such, one or ordinary skill in the art would not combined the references as suggested by the Examiner.

There is no teaching in the prior art of connecting multiple IDE devices to multiple USB-to-

IDE bridges that are connected to a USB controller. For at least these reasons, it is respectfully submitted that not prima facie case of obviousness has been established.

Further, Harris does not disclose that its bridge provides protocol conversion that is even useable in a system were multiple bridges with IDE devices are connected to a USB controller as claimed herein. According to the present invention, when a disk drive 12 with IDE to USB connector 18 is connected to the USB controller/bus, the root hub senses the presence of the new device and initially communicates with the device on e.g. "pipe 0," the default physical device communications channel. Pipes are the data sub-bands of the hub architecture that maintain the physical connections of devices. Once a device is recognized, the root hub interrogates the device to find out what it is and what it is capable of on pipe 0. All of the devices 12 on the USB to IDE ports/connectors 18 are then enumerated and each is assigned a unique device number, which also includes a corresponding pipe number for physical device communications. The host 20 loads the program instructions to control the devices 12 and handles its information flow. The hubs 16 are then running and information is passed in and out of the USB controller 18 via the signal leads. Such is not disclosed by Harris, and shows that Harris cannot be modified to be useable in a system were multiple bridges are connected to a USB controller as claimed herein.

Accordingly, for at least these reasons, rejection of Claim 1, and all claims dependent therefrom, should be withdrawn.

As per **Claim 19**, Harris does not disclose a carrier for each IDE data storage device, such that each IDE disk drive and corresponding USB-to-IDE bridge are stored in the respective carrier. Fig. 3 of Harris (relied on by the Examiner) does not disclose that an IDE disk drive an corresponding USB-to-IDE bridge are stored in a carrier. Fig. 3 of Harris only shows a mass storage circuit board that carries the bridge chip 100 and disk drive *electronics*, not a storage device itself, such as disk drive, as required by Claim 19.

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Despite the Examiner's contention, Harris paragraphs 3-4 are not related to board 20a in Fig. 3 of Harris. Paragraphs 3-4 discuss prior art board 20 in Fig. 1, which Harris criticizes, and Paragraphs 3-4 or board 20 does not disclose a carrier for each IDE data storage device, such that each IDE disk drive and corresponding USB-to-IDE bridge are stored in the respective carrier, as required by Claim 19. In Harris, Fig. 3 and paragraphs 17, 18, 21, 22, 26 which refer to board 20a, there is no disclosure or teaching of the claimed limitations.

Indeed in paragraph 18, Harris states that: "The secondary board 25 and improved mass storage device motherboard 20a, according to these preferred embodiments of the invention, can be used to facilitate more efficient communication *between a host motherboard and a hard drive*, magneto optical drive, CD drive, CD-RW drive, DVD-RAM drive, DVD+RW drive, or any other mass storage device or combination of mass storage devices." (emphasis added). As is glaringly clear from this passage, the board 20a (along with board 25) is between a host motherboard and a drive. The board 20a is not a carrier for a drive. Harris does not disclose or require that board 20a (or board 20 in FIG. 1) carry a drive. No prima facie case of obviousness has been established.

As per **Claim 3**, Harris and Talati do not disclose one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and a USB controller, as claimed. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. If the claims are once again rejected, Applicant respectfully request that the Examiner point to disclosure in the references that teach one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and a USB controller, as required by Claim 3.

As per **Claim 5**, Harris does not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be connected/disconnected to/from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner)

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says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 6**, Harris and Talati do not disclose that at least a third IDE device coupled to a corresponding USB-to-IDE bridge that is connected to a USB controller, can be connected/disconnected to/from the USB controller while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting a third IDE device that is connected to bridges that is connected to a USB controller, as claimed.

As per **Claim 7**, Harris and Talati do not disclose at least one USB hub connected between a number of the USB-to-IDE bridges and the USB controller whereby the processor can communicate with the IDE devices via the USB controller and the USB hub. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs.

As per **Claim 8**, Harris does not disclose that one or more IDE devices can be disconnected from the system while the system is operating. Harris does not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 9**, Harris and Talati do not disclose that at least one additional IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the hub while the system is operating. Harris does not disclose that IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting devices that are

connected to bridges that are connected to a USB controller. Talati and Harris are silent on USB hubs. Items 102 and 104 in Fig. 1 of Talati are not USB hubs as claimed (Talati says nothing about using USB or USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. As such, Harris and Talati do not disclose that at least one additional IDE device coupled to a corresponding USB-to-IDE bridge can be connected to the hub while the system is operating

Claim 10 was rejected for essentially the same reasons as rejection of Claim 1. For at least the reasons provided in relation Claim 1, it is respectfully submitted that Claim 10 and all claims dependent therefrom should be allowed.

As per **Claim 12**, Harris does not disclose hot plugging/unplugging one or more IDE devices that are connected to bridges that are connected to a USB controller. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about hot plugging/unplugging one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 13**, Harris and Talati do not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be connected/disconnected to/from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 14**, Harris and Talati do not disclose that at least a third IDE device coupled to a corresponding USB-to-IDE bridge that is connected to a USB controller, can be connected/disconnected to/from the USB controller while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting a third IDE device that is connected to bridges that is connected to a USB controller, as claimed.

As per **Claim 15**, Harris and Talati do not disclose providing at least one USB hub,

connecting each hub to a USB controller, and connecting two or more USB-to-IDE bridges to each hub, such that each hub is connected between a USB controller and two or more USB-to-IDE bridges. There is no disclosure in the references of at least one USB hub connected between a number of the USB-to-IDE bridges and the USB controller. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs.

As per **Claim 16,** Harris and Talati do not disclose disconnecting one or more of the IDE devices from the system while the system is operating. Harris and Talati does not disclose that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

Claim 18 was rejected for the same reasons as rejection of Claim 1. As such, Claim and claims dependent therefrom should be allowed for at least the reasons provided in relation to Claim 1.

As per **Claim 20,** Harris and Talati do not disclose that one or more IDE storage devices can be disconnected from the system while the system is operating. The references do not disclose that that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 21,** Harris and Talati do not disclose that at least a third IDE disk device coupled to a corresponding USB-to-IDE bridge can be connected to the USB controller while the

system is operating. The references do not disclose that at least a third IDE device coupled to a corresponding USB-to-IDE bridge can be connected to a USB controller, while the system is operating. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting a third IDE device that is connected to a bridge that is connected to a USB controller, as claimed.

As per **Claim 22**, Harris and Talati do not disclose at least one USB hub connected between a number of the USB-to-IDE bridges and the USB controller, whereby the processor can communicate with the IDE devices via the USB controller and the USB hub. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs.

As per **Claim 23**, Harris and Talati do not disclose one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and the USB controller. Items 102 and 104 in Fig. 1 of Talati (relied upon by the Examiner) are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. If the claims are once again rejected, Applicant respectfully request that the Examiner point to disclosure in the references that teach one or more USB hubs, each USB hub connected between two or more USB-to-IDE bridges and a USB controller, as required by Claim 23.

As per **Claim 24**, Harris and Talati do not disclose that at least one or more IDE storage devices can be disconnected from the system while the system is operating. The references do not disclose that that one or more IDE devices that are connected to bridges that are connected to a USB controller, can be disconnected from the system while the system is operating, as claimed. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting/disconnecting

one or more devices that are connected to bridges that are connected to a USB controller, as claimed.

As per **Claim 25**, Harris and Talati do not disclose at least one additional IDE storage device coupled to a corresponding USB-to-IDE bridge can be connected to one of the USB hubs while the system is operating. As discussed, neither Harris nor Talati mention USB hubs, or use of USB hubs. Items 102 and 104 in Fig. 1 of Talati are not USB hubs as claimed (Talati says nothing about using USB or USB hubs). Items 102 and 104 are PHY controllers providing PHY layer protocol connection, not USB hubs. Nor does Harris mention use of USB hubs or need to USB hubs. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting an additional IDE device to a corresponding USB-to-IDE bridge to one of the USB hubs while the system is operating.

As per **Claim 26**, the references do not disclose that at least one additional IDE storage device coupled to a corresponding USB-to-IDE bridge and associated hub, can be connected to the USB controller while the system is operating. As discussed, the references are silent on USB hubs. Further, the references do not disclose an arrangement that comprises an IDE device connected to a USB-to-IDE bridge connected to a USB hub. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about connecting such an arrangement to a USB controller in mid system operation.

As per **Claim 27**, the references do not disclose that at least one IDE storage device coupled to a corresponding USB-to-IDE bridge and associated hub, can be disconnected from the USB controller while the system is operating. As discussed, the references are silent on USB hubs. Further, the references do not disclose an arrangement that comprises an IDE device connected to a USB-to-IDE bridge connected to a USB hub. Paragraph 25 of Harris (relied upon by the Examiner) says nothing about disconnecting connecting such an arrangement from a USB controller in mid system operation.

Rejections of Claims 2, 4 and 11 Under 35 USC 103(a)

Rejection of Claims 2, 4, 11 under 35 U.S.C. 103(a) as being unpatentable over Harris in view Talati and further in view of Abramson is respectfully traversed since for at lese the following reasons, the references alone of in combination, do not disclose all of the claimed limitations.

As per **Claim 2**, as discussed Harris and Talati do not disclose all of the limitations of base Claim 1. Further, as the Examiner also states Harris and Talati do not disclose all of the limitations of Claim 2.

The Examiner interprets Abramson (Fig. 1, 130) as showing a USB controller connected to a processor via a PCI bus. This interpretation of Abramson is respectfully traversed. In Fig. 1 of Abramson, the processor 105 is not connected to a PCI bus, rather the processor 105 is connected to the host bridge 115 via host bus 110.

Further, in Abramson the PCI bus 130 is not connected to any USB controller. Rather, the PCI bus 130 is connected to the host bridge 115, the bus interface unit 140 and the devices 135, none of which are USB controllers. A USB controller 150 is in a USB dual host controller chip 139, but the USB controller 150 has units 145 and 150 between it and the PCI bus 130.

As such, one of ordinary skill in the art would not look to the references to achieve the solution provided by the present invention. Further, the references themselves do not suggest a motivation for the combination suggested by the Examiner. A PCI bus is not even mentioned in Harris or Talati.

As per **Claim 4**, as discussed Harris and Talati do not disclose all of the limitations of base Claim 1. In addition, Harris, Talati and Abramson do not disclose a plurality of USB controllers connected to the processor, wherein one or more USB-to-IDE bridges are connected to each USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for

communication between the corresponding IDE device and that USB controller, whereby the processor can communicate with the IDE devices via the USB controllers, as claimed.

Further, despite the Examiner's interpretation, it is respectfully submitted that Harris (paragraph 9, relied on by the Examiner) does not disclose one or more USB-to-IDE bridges are connected to each USB controller via a USB bus, each USB-to-IDE bridge providing protocol conversion for communication between the corresponding IDE device and that USB controller, whereby the processor can communicate with the IDE devices via the USB controllers. Harris, paragraph 9, simply states that: "Alternatively, a secondary board could be used to provide the translation function. In this embodiment, the secondary board includes the bridging circuit for converting ATA/ATAPI signals to USB signals. The secondary board receives the ATA/ATAPI signals from a mass storage device motherboard and outputs USB signals to the host motherboard." This is simply discussing placing the bridge circuit on one board and the disk drive electronics on another board. This has nothing to do with the claimed limitations. The Examiner has not addressed this point in the office action at all.

Further, as the Examiner states, Harris and Talati do not disclose a plurality of USB controllers. Abramson (Figure 1) does no show a plurality of USB controllers connected to the processor 105, as claimed. As mentioned, the USB controllers 150, 155 must go through arbitration 145, as a result of which only one of the units 150, 155 at a time can communicate with the interface 140. As such, there is no case in Abramson wherein a plurality of USB controllers are connected to the processor, wherein one or more USB-to-IDE bridges and corresponding IDE devices are connected to each USB controller via a USB bus, whereby the processor can communicate with the IDE devices via the USB controllers, as claimed.

There is no mention in Abramson of multiple USB controllers connected to the processor, to each of which multiple USB-to-IDE bridges are connected, wherein the processor communicates with the IDE devices via the controllers and the bridges.

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There is no motivation or suggestion by the references to combine them. There is no disclosure or suggestion in the references that a processor can communicate with multiple IDE devices via multiple bridges via a plurality of USB controllers. The Examiner has not explained how the systems in the three references can be combined without extensive modification. It is respectfully submitted that the Examiner is simply using hindsight.
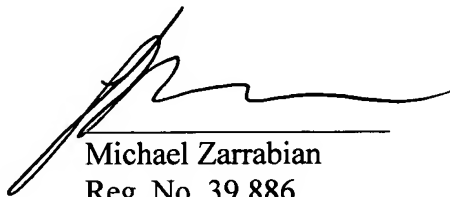
Claim 11 was rejected for the same reasons as rejection of Claim 2, and should therefore be allowed for at least the reasons provided in relation to Claim 2.

CONCLUSION

For the foregoing, and other, reasons Applicants believe that the rejected claims should be allowed. Reconsideration and allowance of the rejected claims are respectfully requested.

Please continue to direct all communications regarding the above-referenced patent application to the principal agent of record.
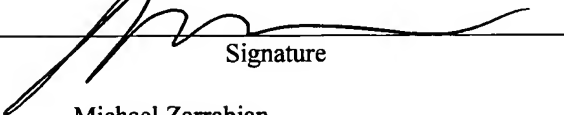
Respectfully Submitted,

Michael Zarrabian
Reg. No. 39,886

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